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... of the actual interleaving of the instructions executed ... Direct execution was frequently

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... a solution to the instruction-set compatibility ... translation provides machines with

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JH Edmondson, P Rubinfeld, R Preston, V ... - Micro, IEEE, 1995 - ieeexplore.ieee.org

... in the memory unit and a 48 entry instruction translation buffer in the instruction

unit. ... The integer and floating-point execution units are 6's- hits wide ...

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... system kernel, and the hardware simulator run together in a ... sor workstation, including

CPU instruction execution, address translation, interrupts, and ...

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## Some efficient architecture simulation techniques - group of 11 »

R Bedichek - Winter 1990 Usenix Conference, 1990 - xsim.com

... Execution of delayed branches cause the decoded ip to be ... from the presence of a stale

translation in the ... limit on the number of decoded instruction pages that ...

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PS Magnusson, F Dahlgren, H Grahn, M Karlsson, F ... - Proceedings of the 1998 USENIX Annual Technical Conference, 1998 - usenix.org

... benefit of running within a simulator is that ... read cache misses (data) (d) translation

look-aside ... the instruction (g) count of instruction execution (h) flag ...

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Douglas W. Clark, Joel S. Emer

February 1985 ACM Transactions on Computer Systems (TOCS), Volume 3 Issue 1

Publisher: ACM Press

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A virtual-address translation buffer (TB) is a hardware cache of recently used virtual-tophysical address mappings. The authors present the results of a set of measurements and simulations of translation buffer performance in the VAX-11/780. Two different hardware monitors were attached to VAX-11/780 computers, and translation buffer behavior was measured. Measurements were made under normal time-sharing use and while running reproducible synthetic time-sharing work loads. Reported measure ...

2 Efficient instruction cache simulation and execution profiling with a threaded-code



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Peter S. Magnusson

December 1997 Proceedings of the 29th conference on Winter simulation

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Embra: fast and flexible machine simulation



Emmett Witchel, Mendel Rosenblum

May 1996 ACM SIGMETRICS Performance Evaluation Review, Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '96, Volume 24 Issue 1

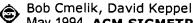
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This paper describes Embra, a simulator for the processors, caches, and memory systems of uniprocessors and cache-coherent multiprocessors. When running as part of the SimOS simulation environment, Embra models the processors of a MIPS R3000/R4000 machine faithfully enough to run a commercial operating system and arbitrary user applications. To achieve high simulation speed, Embra uses dynamic binary translation to generate code sequences which simulate the workload. It is the first machine simu ...

Shade: a fast instruction-set simulator for execution profiling



May 1994 ACM SIGMETRICS Performance Evaluation Review , Proceedings of the